CLAIMS:

What is claimed:

1. In a method for designing a circuit where design parameters for performance specifications are represented by posynomial expressions with constraints and solved with geometric programming, an improvement for simultaneously determining the boundaries for circuit elements in the floorplan of the circuit comprising:

representing the boundaries for circuit elements in the floorplan of the circuit as posynomial expressions with constraints on circuit size;

solving the posynomial expressions for the design parameters and floorplan boundaries on a digital computer using geometric programming;

outputting the results in a format that can be used by a circuit designer in the fabrication of the circuit.

2. The method defined by claims 1 wherein the representation of the floorplan of the circuit includes the slicing of the circuit along the boundaries of the circuit elements.

3. The method defined by claim 1 or 2 including using layout constraints for the floorplan.

4. The method defined by claim 3 wherein one layout constraint is a limitation on the circuit area.

5. The method defined by claim 4 wherein another layout constraint is a limitation on the aspect ratio of the circuit layout.

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6. In a method for designing an analog integrated circuit having active circuit elements where design parameters for performance specifications are represented by posynomial expressions with constraints and then solved with geometric programming, an improvement for simultaneously determining the boundaries for the active circuit elements in a floorplan for the integrated circuit comprising:

representing the floorplan as posynomial constraints of vertical and horizontal dimensions for each of the active circuit elements;

solving the posynomial expressions for the design parameters and vertical and horizontal dimensions; and

outputting the results of the preceding step in a format usable for a circuit designer to fabricate the integrated circuit.

7. The method defined by claim 6 wherein the integrated circuit is sliced vertically and horizontally along the boundaries of the circuit elements.

8. The method defined by claim 7 wherein for a vertical slice, the resulting first sibling nodes are represented by a sum of horizontal dimensions of the first sibling nodes being equal to or less than a first parent node and which dimensions of the first sibling nodes each being equal to or less than a vertical dimension of the first parent node.

9. The method defined by claim 8 wherein for each horizontal slice, the resulting second sibling nodes are represented by the sum of the vertical dimensions of the second sibling nodes being equal to or less than a second parent node, and the horizontal dimensions of second sibling nodes each being equal to or less than a vertical height of the second parent node.

10. The method defined by claim 6 or 9 wherein the circuit elements include MOS transistors where the vertical dimension and horizontal dimension of each of the MOS transistors is represented by a posynomial expression.

11. The method defined by claim 10 wherein the posynomial expression for the vertical and horizontal dimensions of the MOS transistors include process dependant parameters.

12. The method defined by claim defined by claim 11 wherein the design of the analog circuit presupposes that the active circuit elements are operating in their saturation regions.